On-chip Si-based Bragg cladding waveguide with high index contrast bilayers

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Abstract: A new silicon based waveguide with full CMOS compatibility is developed to fabricate an on-chip Bragg cladding waveguide that has an oxide core surrounded by a high index contrast cladding layers. The cladding consists of several dielectric bilayers, where each bilayer consists of a high index-contrast pair of layers of Si and Si_3N_4. This new waveguide guides light based on omnidirectional reflection, reflecting light at any angle or polarization back into the core. Its fabrication is fully compatible with current microelectronics processes. In principle, a core of any low-index material can be realized with our novel structure, including air. Potential applications include tight turning radii, high power transmission, and dispersion compensation.

OCIS codes: (130.2790) Guided waves; (160.3130) Integrated optics materials

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1. Introduction

Recently, interest in guiding light within low-index materials (including air) has increased, with new devices that use a Bragg reflection [1-5] or photonic band gap (PBG) [6-8] to confine light. Specific examples include 2D photonic crystal fibers [9-11] and ARROW waveguides [12]. Another example, the omniguide fiber, uses high index contrast concentric dielectric layers to enhance the mode confinement in a relatively simple structure [13-15]. It is difficult to fabricate this structure on a silicon chip. However, the same principle of using 1D omnidirectional mirrors can be applied to an alternative structure that can be fabricated with current microelectronics technology processes (CMOS compatible processes). Toward that end, an on-chip silicon-based Bragg cladding waveguide is designed with low refractive index material for the core, and stratified high index contrast dielectric layers as the cladding. Due to the high index contrast of these materials with each other, they have a large photonic band gap, and may act as omnidirectional reflectors, which means light of all incident angles and polarizations is reflected within a range of wavelengths (e.g., near 1550 nm). In contrast with an index-guided waveguide (e.g., SiO_xN_y), it is possible to confine light to a low index core (possibly air) on chip. The high index contrast allows the cladding thickness to be less than 2 microns, which is much thinner than the conventional silica optical bench waveguide.

The on-chip Bragg waveguide is designed with a low index core layer of SiO_2 (n=1.46) and a high index contrast cladding consisting of pairs of layers of Si (n=3.5) and Si_3N_4 (n=2.0), which each have a quarter wavelength thickness at the target wavelength of 1550 nm. The on-chip Bragg cladding waveguide configuration is illustrated in Fig. 1. It combines the ease of layer-by-layer fabrication (as discussed below) with low losses that are associated with the presence of a highly reflective mirror on all sides of the core. Guided modes and their modal behavior for both polarizations (TE and TM) can be predicted by comparison with a waveguide made from perfectly reflecting metallic walls [16]. The dispersion of the dielectric waveguide matches pretty well with the metallic waveguide, except for one key difference, which is the phase shift associated with reflections from the dielectric surface.

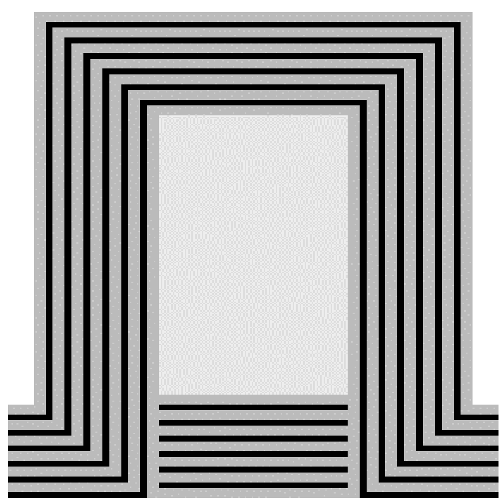

Fig. 1. The illustration of the Bragg cladding waveguide, with low index core (SiO_2) and Si/Si_3N_4 as dielectric cladding layers.

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2. Fabrication and measurements

The on-chip Bragg waveguide is fabricated with a CMOS-compatible process: the Low Pressure Chemical Vapor Deposition (LPCVD) is used to deposit the Si and Si_3N_4 cladding layers and the Low Temperature Oxide (LTO) method is used to make the oxide core. On a 6" Si chip, the 110 nm Si layer is deposited using the LPCVD method at a temperature of 625°C; the 194 nm Si_3N_4 layer is deposited using LPCVD at a temperature of 775°C. After the deposition of the bottom six and a half 1D PBG crystal layers, we use the LTO method to deposit SiO_2 at 450°C, followed by a 900°C anneal, to obtain a high quality oxide layer with a thickness between 4 and 6 microns. Lithography and high-density plasma etching is then used to define the waveguide core geometry. Finally, the same deposition method (LPCVD) is used to finish the top six and a half Si/Si3N4 Bragg cladding layers. Figure 2(a) is a TEM picture of a Bragg cladding slab fabricated using this technique, consisting of 7 layers of Si_3N_4 and 6 layers of poly-Si arranged in a periodic structure, with top SiO_2 layer and on Si substrate. Clearly, the LPCVD deposition method is able to accurately control the thickness and flatness of the Si and Si_3N_4 layers, both of which are important to prevent scattering losses. The high index contrast of the Si and Si_3N_4 pairs gives rise to a large photonic bandgap and high reflectivity (greater than 99%) for only a few bilayers. This is illustrated in Fig. 2(b), where the measured absolute reflectivity of five Si/Si_3N_4 bilayers at normal incidence is compared with a numerical calculation of the reflectivity of the ideal structure, using the transfer matrix method. The measurement and calculation are in very good agreement with each other, most importantly in the stop band, which extends from 1200nm to 2000nm. The spectral range of omnidirectional high reflection is from 1200nm to 1700nm.

A TEM picture of the final product, the fabricated on-chip Bragg cladding waveguide, is shown in Fig. 3(a). For the top Bragg cladding layers, each individual Si and Si_3N_4 layer is smooth, even at the curved surface, which shows the high quality of LPCVD's conformal step coverage. From Fig. 3(a), we conclude that CMOS compatible high and low index materials have good thermal and mechanical properties. The on-chip Bragg cladded waveguide loss is measured at 1550nm using the following procedure: light from a tapered optical fiber is coupled into the waveguide, then the guided light emerging from the other end is focused with a lens and collected with a camera. Figure 3(b) shows the guided spot imaged by the camera, which demonstrates the presence of one or more well-defined guided modes, which are primarily concentrated in the low index SiO_2 core. From the measurement on the waveguide loss using different waveguide length (~ 3mm), the waveguide loss is as low as 6 dB/cm.

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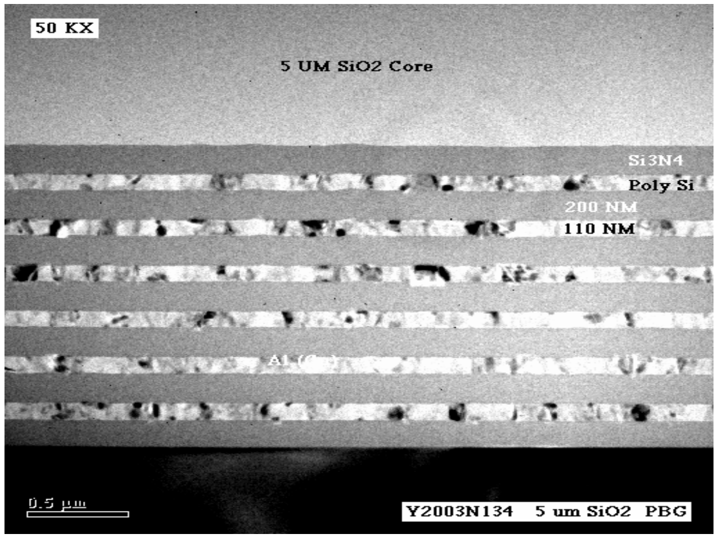
(a)



(b)

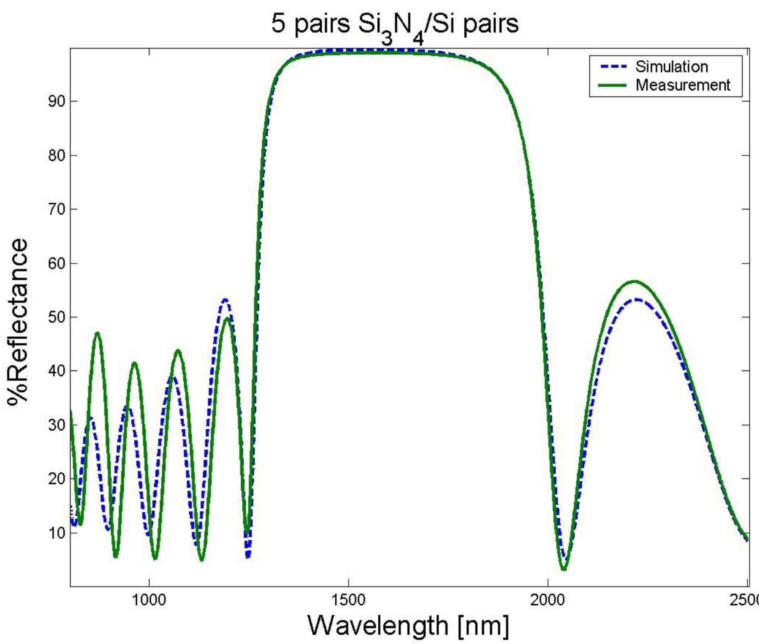


Fig. 2. (a) The TEM image of the cladding pairs including the bottom Bragg cladding layers (Si/Si_3N_4) and SiO_2 core. (b) The measurement and simulation on absolute reflectivity of 5 pairs Si/Si_3N_4 layers.

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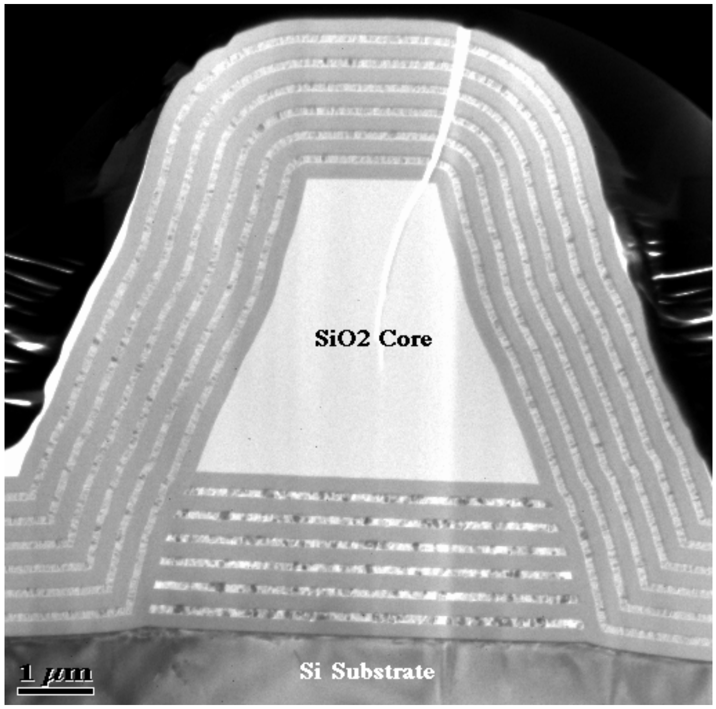
(a)



(b)

Fig. 3. (a) The TEM image of the fabricated Bragg cladded channel waveguide. The smooth interface and good conformal step coverage by LPCVD method are clearly seen. (b) The guided spot from the Bragg cladded channel waveguide with dimension 4µm x4µm, which demonstrated the guidance in the low index SiO_2 materials by PBG guiding mechanism.

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3. Summary

In this work, a SiO_2 core is used in the example of on-chip Bragg cladding waveguide structure. However, fabrication need not be restricted to SiO_2 – a hollow core could also be fabricated with a slight change in the procedure. This so-called "core freedom" would give rise to multiple applications, for example, transmission of high intensity beams (e.g., for a CO_2 laser) through a hollow core without absorption or nonlinearity, or to trap light -- or even modify the rate of emission -- from an optically active material. It also has unique group-velocity dispersion characteristics, which can be modified with changes to the core.

In conclusion, a new Si based Bragg cladded waveguide, whose fabrication is fully compatible to the current CMOS technology, is developed. Si and Si_3N_4 are deposited using LPCVD method and high quality Bragg cladding layers are realized. Light guiding in the low index core is demonstrated. A thin Bragg cladding, made possible by the large index contrast between the Si and Si_3N_4 layers, indicates the advantage of this device over traditional silica optical bench waveguides.

Acknowledgments

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