Fabrication of two-dimensional tungsten photonic crystals for high-temperature applications

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(Received 30 March 2011; accepted 10 September 2011; published 24 October 2011)

This article details microfabrication of two-dimensional tungsten photonic crystals (2D W PhCs) for high-temperature applications such as selective thermal emitters for thermophotovoltaic energy conversion. In particular, interference lithography and reactive ion etching are used to produce large area single crystal tungsten 2D PhCs. For this investigation, we fabricated a 2D W PhC sample consisting of an array of cylindrical cavities with 800 nm diameter, 1.2 μm depth, and 1.2 μm period. Extensive characterization and calibration of all microfabrication steps are presented. Experimentally obtained thermal emissivity spectrum is shown to match well with numerical simulations. © *2011 American Vacuum Society*. [DOI: 10.1116/1.3646475]

I. INTRODUCTION

Two-dimensional metallic photonic crystals are promising as high-performance selective thermal emitters for thermophotovoltaic energy conversion, including solar-thermophotovoltaic and radioisotope-thermophotovoltaic generators,[1] as well as highly efficient solar absorbers/emitters.[2] A number of articles have been published on different designs of tungsten (W) photonic crystals (PhCs) as selective thermal emitters.[3–6] In particular, Sai and co-workers reported the design and fabrication of an array of square cavities in W whereby an expensive and time-consuming fabrication technique based on e-beam lithography and fast atom beam etching were used to fabricate these structures.[5,6] A different selective emitter has also been reported by Lin and co-workers based on the 3D W woodpile stack design,[3,4] which also requires an expensive and complex layer by layer fabrication method. In contrast, the work presented here explores a different approach for fabrication of selective broadband emitters based on interference lithography and reactive ion etching. This process employs standard microfabrication techniques that are relatively simple, efficient, and readily scalable.

Our design is based on 2D W PhCs consisting of a square array of cylindrical holes. Key design parameters that determine thermal emission cutoff and selectivity are radius and depth of the holes, as well as the periodicity. For demonstration purposes, we designed and fabricated a 2D W PhC sample with cylindrical cavities of diameter 800 nm, depth 1.2 μm, and period 1.2 μm using single crystal W as the substrate. This article focuses on key aspects of the fabrication process that enable us to achieve the required dimensional reliability, repeatability, and optical performance.

II. FABRICATION

The fabrication process, schematically shown in Fig. 1, consists of two main parts: lithography and etching. The first step is the deposition of a chromium (Cr) layer on the single crystal W substrate using electron-beam evaporation. This layer is used as the hard mask for the underlying W layer. Next, antireflection coating (ARC) and photoresist (PR) are sequentially spun on top of the Cr layer. After the lithographic exposure, we transfer the desired pattern from one layer to the next layer by various etching processes until we obtain periodic cylindrical holes on the W substrate. The following two sections describe the lithography and etching steps in more detail.

A. Lithography

We use a bi-level resist process in which patterns are imaged and developed on the PR layer over the ARC.[7] After depositing Cr on the single crystal W substrate, we spin cyclohexanone-based BARLi ARC on the sample. The ARC is required to minimize scalloping of the PR sidewalls due to vertical reflected standing waves from the Cr layer. Reflectivity calculations were performed to determine the proper thickness of the ARC layer that results in minimum reflection, and the calculation method is similar to the one used in previous works.[8–10] The THMRiN-PS4 photoresist by OHKA America is then spun on the sample. Next, we use laser interference lithography (IL) to perform the exposure, since it is relatively inexpensive, fast, and precise, while allowing exposure of relatively large sample sizes.[11] IL is a maskless lithography method relying on the interference pattern generated by two coherent light sources, and thus is useful for defining 1D and 2D periodic patterns on a single plane.[11] A detailed description of IL systems and different implementations of this method are discussed in Ref. 11. Instead of having two lasers, we used Lloyd's mirror IL system, which is among the simplest of IL systems,[12] which includes a mirror mounted at 90° angle to the substrate to be exposed. The interference lithography setup is shown in Fig. 2. A helium–cadmium (HeCd) laser emitting at 325 nm is used as the source of coherent illumination as shown in Fig. 2. The long (2 m) separation between the source and the

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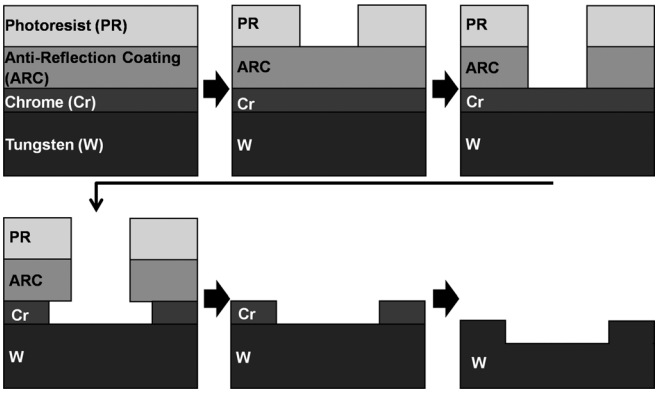

FIG. 1. General process flow: After depositing a layer of Cr on the W substrate, lithography layers consisting of the ARC and the PR are coated on the Cr. After lithographic exposure, the desired pattern is transferred from the one layer to the next layer by various etching processes until periodic cylindrical holes on the W substrate are obtained.

sample provides the necessary approximate plane wave incidence at the sample surface.[12]

To achieve a 2D square lattice, two exposures 90° to each other are performed. The proximity effect is responsible for the shape of the holes,[13] resulting in circular holes at longer exposure times and square holes at shorter exposure times. Calibration tests were performed to determine the appropriate exposure times for the desired shape of the hole. For obtaining a square hole, the minimum exposure time required was 35 s at a laser power of 170 μW in the plane of the sample. For a circular hole, it is necessary to have a longer exposure time, which in our case is 90 s. This is illustrated in Fig. 3. The relationship between the exposure time and the pitch of the structure, defined as the ratio of the hole diameter to structure period, is shown to be approximately linear.

Due to the use of negative tone photoresist, we are limited to either round holes with thick sidewalls or square holes with thin sidewalls as shown in Fig. 3. It is not possible to satisfy both at the same time. Preserving the round shape of the holes is the main priority, since the holes can be easily widened to the desired diameter in the Cr wet etch step, which we detail later. Hence, in the lithography step, overexposure is favored in producing a square array of circular

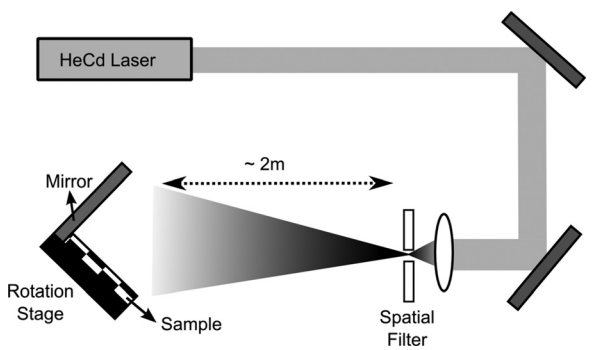

FIG. 2. Schematics of the laser interference lithography used in exposing the photoresist.

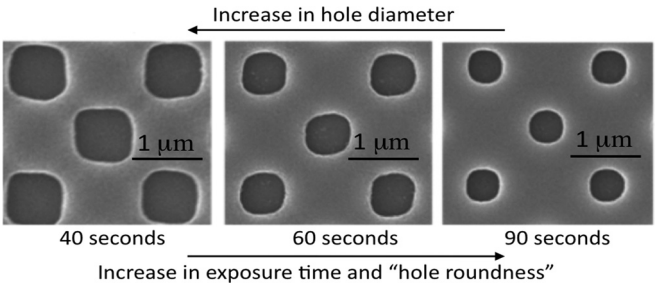

FIG. 3. SEM images of the developed patterns in the photoresist for different exposure times, whereby the laser power is 170 μW at the sample plane.

holes. After the lithography step, the PR is then developed in the commercial CD-26 developer. In the following, the etching processes of ARC, Cr, and W are described.

B. Etching

1. ARC etching

In order to transfer the pattern from the PR to the ARC, oxygen based reactive ion etching (RIE) is performed using the Plasma-Therm 790 Series RIE System. To preserve the hole size without widening the hole, it is important to only etch for the minimum required time such that no ARC remains, i.e., until the Cr layer is completely exposed. Hence, a number of RIE calibration experiments were conducted to determine conditions necessary to ensure that the ARC is etched completely. For our particular RIE system, we determine that a 2:1 (10 sccm:5 sccm) mixture of helium and oxygen under a process pressure of 7 mTorr and 250 V bias works well. Figure 4 shows the ARC layer after RIE with RF power of 140–145 W at 3 min and 30 s, which does not show any residual ARC in the holes. In contrast, a 3 min long etch resulted in residual ARC in the holes.

2. Chromium etching

In order to etch the Cr hard mask layer, Cyantek CR-7, a commercially available Cr wet etchant manufactured by Cyantek Corporation is used. The CR-7 etchant is diluted with 40% distilled water to slow down the etch rate; thus

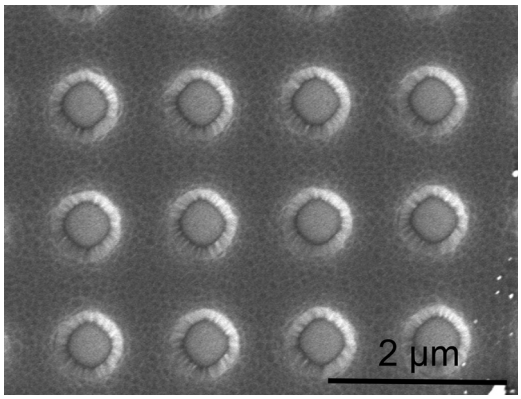

FIG. 4. SEM image showing successful pattern transfer to the antireflection coating after undergoing oxygen based reactive ion etching at 140 W for 3 min and 30 s.

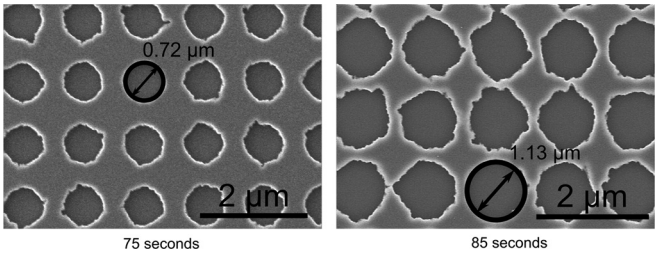

FIG. 5. SEM images demonstrating the control of etch times to obtain the desired circular hole average diameter on the chromium mask.

allowing superior control and repeatability of reaction time vital in adjusting and obtaining the desired diameter of the holes. This is illustrated in Fig. 5. Note that excessive etch times lead to breaking of the sidewalls. The ARC layer is then removed using the same ARC RIE process described earlier.

The quality of the Cr mask is important to ensure the etch is uniform and the sidewalls are smooth. During the Cr mask deposition, it is important to achieve high quality vacuum (<0.01 mTorr). Increasing the substrate temperature to 250 °C during the deposition results in more uniform etching, which we believe is due to better quality of deposited Cr. Figure 6 shows the comparison of etched Cr mask deposited at high temperature and at room temperature. As shown in Fig. 6, high-temperature deposition results in smoother sidewalls and a more uniform etch.

3. Tungsten etching

The final step is the W etch. We used a 6.7:1 carbon tetrafluoride (CF_4) to oxygen (16 sccm: 2.4 sccm) based RIE process to transfer the pattern from the Cr hard mask layer into the W substrate. The final etch depth is determined by both the etch rate and the thickness of Cr mask. The etch rate is related to the ratio of the gases, pressure, and power used in the RIE process. Table I compares the experimental observation for different powers and pressures, and their advantages and disadvantages. It is observed that for etches longer than 5 min, the etch saturates, which is due to the nature of our RIE system. Therefore, incremental etch steps of 5 min were used.

The Cr mask thickness is slowly reduced during the W RIE process. Experimental results show that for every 10 nm of W, approximately 1 nm of Cr is sputtered away. However,

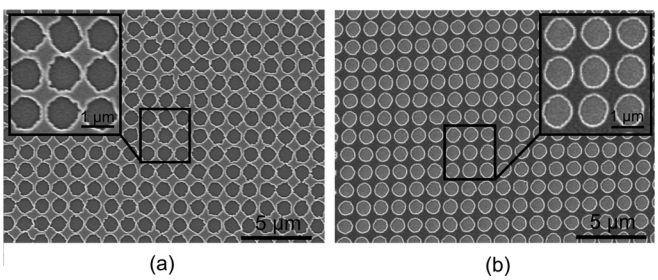

FIG. 6. Chrome mask after lithography steps. Prior to lithography, chrome deposition was performed at (a) room temperature and (b) high temperature (250 °C).

TABLE I. Different RIE etch parameters and their effects on etch rate and mask damage.

Power (W)	90	90	108
Pressure (mTorr)	10	7	10
Etch depth (%)	100	84	120
Remaining Cr (%)	20	30	0
Mask damage	Little	Little	High
Etch rate	Medium	Low	High

this relationship is not exactly linear. The Cr mask is initially very durable, but erodes with prolonged exposure to the W RIE process. For our experiment, 120 nm of Cr enabled a W etch depth of approximately 1.2 μm.

III. DESIGN AND CHARACTERIZATION

A. Design

Previous work has demonstrated that the enhancement of the thermal emission of 2D W PhCs is achieved by coupling into the resonant modes of the periodic cylindrical cavities.[14] In such a cavity, the resonant frequency is found to be strongly dependent on the radius and hole depth. Hence, by

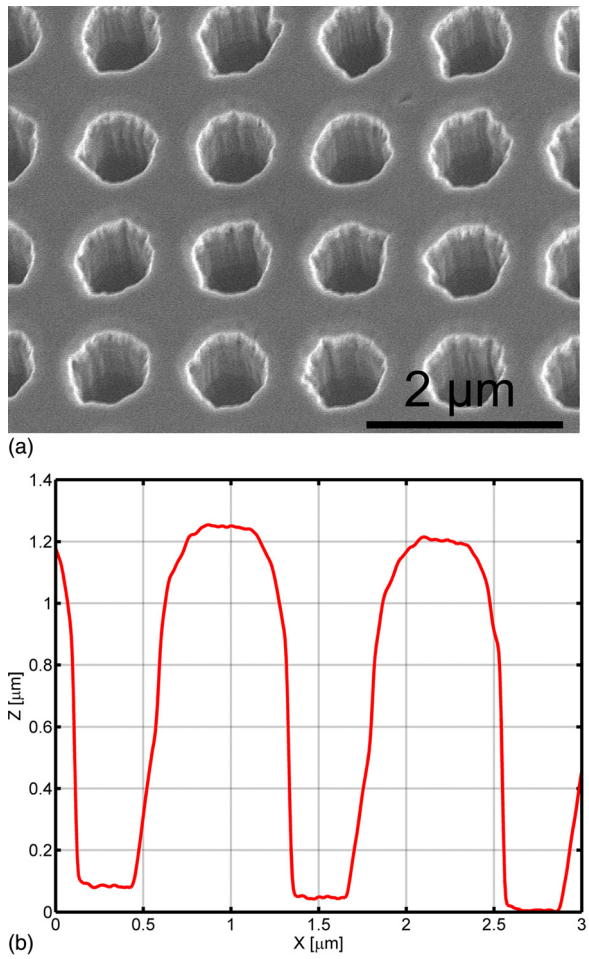

FIG. 7. (Color online) (a) SEM image of the final 2D W PhC and (b) cross-sectional profile mapped using an AFM.

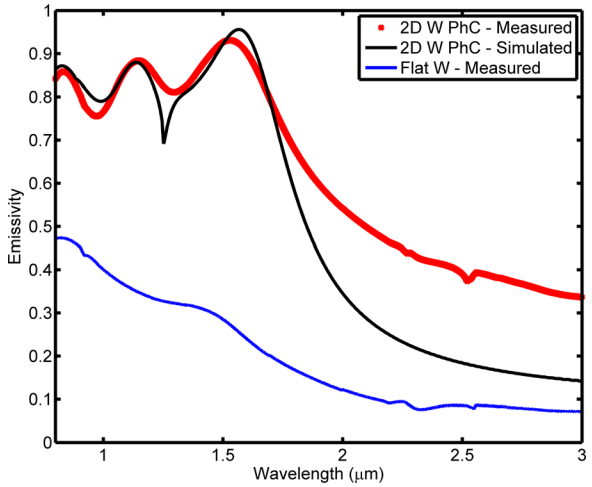

FIG. 8. (Color online) A marked enhancement is seen in the emissivity of the 2D W PhC at wavelengths below 1.7μm.

varying the radius and depth of holes, one can tailor the resonant frequencies to suit various applications. More important, the peak emittance can be maximized via Q matching through the control of depth. Therefore, it is important to achieve good control over the parameters during fabrication.

To demonstrate the fabrication process, we designed a 2D W PhC thermal emitter that has a cutoff near the wavelength of 1.7 μm suitable for gallium antimonide based thermophotovoltaics. Finite difference time domain simulations show that a 2D W PhC with cylindrical cavities of diameter 800 nm, depth 1.2 μm, and period 1.2 μm is suitable. This is fabricated following the process described in Sec. II.

B. Characterization

Figure 7 shows the scanning electron micrograph (SEM) of the final 2D W PhC as well as the cross-sectional profile measured using an atomic force microscopy (AFM). As can be seen, we achieved our target depth of 1.2 μm, diameter of 800 nm, and period of 1.2 μm for a circular sample with 10 mm diameter. To evaluate the performance of the fabricated 2D W PhC, we measured its room temperature reflectance using a dual-beam spectrophotometer (Cary 5E UV-VIS-IR). Furthermore, we calculate its absorptivity, upon which the emissivity can then be implied by virtue of Kirchhoff's law. The results are shown in Fig. 8. As can be seen, a substantial improvement in the emissivity is observed below the cutoff wavelength of 1.7 μm compared to that of the flat W. In particular, the measurements match well with the calculated spectra in terms of the resonant peaks. However, the emissivity above the cutoff wavelength is measured to be much higher. This is primarily due to surface contamination; a high concentration of Cr, fluorine, and oxygen remained on the top surface of the PhC as determined by x-ray photoelectron spectroscopy. Cr is much more absorptive than W at those wavelengths; thus severely elevating long wavelength emissivity. We believe that the excessive exposure to etching resulted in Cr compounds that are difficult to remove by the Cr-7 wet etchant in the final mask removal step. This, however, can be easily circumvented by depositing a thicker Cr layer for the same etch times. In addition, the elevated long wavelength emissivity is also caused by the breaking of the sidewalls, which allows longer wavelength photons to interact with the cavities. This effect can be minimized by increasing the period slightly to allow for the stochastic nature of the wet etch.

IV. CONCLUSION

We have developed a method to fabricate two-dimensional tungsten photonic crystals for high-temperature applications. Our fabrication method is based on standard silicon processing techniques that are simple, efficient, and easily scalable. Using finite difference time domain simulations, we designed and fabricated a 2D W PhC with cylindrical cavities of diameter 800 nm, depth 1.2 μm, and period 1.2 μm. This structure has a cutoff near the wavelength of 1.7 μm. A marked enhancement is measured in the emissivity of the 2D W PhC at wavelengths below 1.7 μm compared to flat W. The measurements match well with the calculated spectra in terms of the resonant peaks.

ACKNOWLEDGMENTS

The authors thank Jim Daley for film deposition and sample preparation. This work was supported in part by the MRSEC Program of the National Science Foundation under Award No. DMR-0819762, the MIT S3TEC Energy Research Frontier Center of the Department of Energy under Grant No. DE-SC0001299, and the Army Research Office through the Institute for Soldier Nanotechnologies under Contract Nos. DAAD-19-02-D0002 and W911NF-07-D0004.

[1]C. J. Crowley, N. A. Elkouh, S. Murray, D. L. Chubb, in *Space Technology and Applications International Forum*, edited by M. S. El-Genk and M. J. Bragg (AIP, Albuquerque, NM, 2005).
[2]V. M. Andreev, A. S. Vlasov, V. P. Khvostikov, O. A. Khvostikova, P. Y. Gazaryan, S. V. Sorokina, and N. A. Sadchikov, J. Sol. Energy Eng. **129**, 298 (2007).
[3]S. Y. Lin, J. G. Fleming, and I. El-Kady, Opt. Lett. **28**, 1683 (2003).
[4]S. Y. Lin, J. Moreno, and J. G. Fleming, Appl. Phys. Lett. **83**, 380 (2003).
[5]H. Sai, Y. Kanamori, and H. Yugami, Appl. Phys. Lett. **82**, 1685 (2003).
[6]H. Sai and H. Yugami, Appl. Phys. Lett. **85**, 3399 (2004).
[7]T. A. Savas, Satyen N. Shah, M. L. Schattenburg, J. M. Carter, and Henry I. Smith, J. Vac. Sci. Technol. B **13**, 2732 (1995).
[8]M. L. Schattenburg, R. J. Aucoin, and R. C. Fleming, J. Vac. Sci. Technol. B **13**, 3007 (1995).
[9]T. A. Savas, M. L. Schattenburg, J. M. Carter, and Henry I. Smith, J. Vac. Sci. Technol. B **14**, 4167 (1996).
[10]M. G. Moharam, Drew A. Pommet, Eric B. Grann, and T. K. Gaylord, J. Opt. Soc. Am. A **12**, 1077 (1995).
[11]Michael E. Walsh, "On the design of lithographic interferometer and their application," Ph.D. thesis(MIT, Cambridge, 2004).
[12]Thomas B. O'Reilly and Henry I. Smith, J. Vac. Sci. Technol. B **26**, 2131 (2008).
[13]W. Bogaerts, V. Wiaux, D. Taillaert, S. Beckx, B. Luyssaert, P. Bienstman, and R. Baets, IEEE J. Quantum Electron. **8**, 928 (2002).
[14]Ivan Celanovic, Natalija Jovanovic, and John Kassakian, Appl. Phys. Lett. **92**, 193101 (2008).